ISSN 2664-4150 (Print) & ISSN 2664-794X (Online)
South Asian Research Journal of Engineering and Technology
Abbreviated Key Title: South Asian Res J Eng Tech

| Volume-1 | Issue-4 | Nov-Dec -2019 | **DOI: 10.36346/sarjet.2019.v01i04.002**

Review Article

Comparative Analysis of Nano Scale Approximate Adder for Low Leakage Arithmetic Application

Divesh Kumar[1*], Jeba Shalin[1]

[1]EE Department, Bhai Gurdas Institute of Engineering and Technology, Sangrur, India

***Corresponding Author**
Divesh Kumar

Article History
Received: 24.11.2019
Accepted: 15.12.2019
Published: 30.12.2019

Abstract: Low power is the prime requirement to design power efficient VLSI circuits for portable electronic system. This paper presents a two modified approximate adder at 45nm technology. Performance of proposed adder is evaluated in terms of power dissipation, power delay product and compared with conventional full adder design. All the simulations are carried out using 45nm technology at 1.1v supply voltage at 500MHzas well as 1 GHz frequency. It can be seen from the results that leakage power reduces 71% for 1-bit approximate adder and energy consumption reduces upto82% while having dynamic power dissipation in acceptable range with marginal increase in delay.

Keywords: PDP (Power Delay Product), CMOS (Complementary metal oxide semiconductor), VLSI (Very Large Scale Integration).

1. INTRODUCTION

As the demand of portable electronic devices are driving the designers to strive for higher speed, long battery life and more reliable designs [1]. Recently, an overwhelming interest has been seen in the problem of designing digital system with low power at no performance penalty.

The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP) [2], therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to increasing density of chip. Therefore, in realizing modern Very Large Scale integration (VLSI) circuits, low power and high speed [3] are the two predominant factors which need to be considered. Like any other circuits design, the design of high performance and low power adders can be addressed at different levels, such as architecture, logic style, and layout and process technology. As the result, there always exist a trade-off between the design parameter such as speed, power consumption and area. As, each computational circuit is incomplete without an adder. It has become a common aim to decrease the power consumption and delay of these adder cells. There are various techniques to minimize power consumption and maximizing the battery life. Power gating is one among them in which a sleep transistor is placed in between real ground rail and virtual ground (circuit ground) [4]. This approach reduces the leakage power and ground bounce noise with minimum impact on performance of circuit .Two output load capacitances are used to measure dynamic power and delay [5].

Recently, approximation is attracting researchers for designing low leakage circuits for large arithmetic applications because there are number of image processing applications where strict exactness is not required. Even if there are wrong output upto three or four data combinations in full adder, then also it can be satisfactory used in image processing applications [6]. We have proposed two basic design of approximate adder, which can be utilized efficiently in DSP blocks [7]. Our proposed design is having best performance parameters with improved leakage power dissipation.

2. Previous Work

On the basis of requirements such as area, delay and power consumption, different types of recent adders. Some of the recently published techniques are reviewed in this section. R. Jothin *et al.*, [7] presented the modified technique of approximate computing at architecture level which is known as static segment adder. It which improves the overall

performance based on static segmentation but energy consumption is not optimized another approximate adders [8] is presented the design of approximate adder for low-power computations. In many applications, completely correct results are not required. Approximate adder structure consists of four blocks each of four bits. Lower 8-bits are computed by two imprecise blocks and two conventional adder computes the higher 8-bits. Although there is improvement in performance parameters but leakage power is not optimized. Another design of adder is presented by Z. Guan [7] for high speed and low power arithmetic circuits although there are tremendous improvements in their performance parameters but leakage and energy consumption is not optimized. Similarly R. Singh *et al.,* [8] presented the modeling and analysis of low power 10T full adder with reduced ground bounce noise. Stacking power gating is used to evaluate leakage current, power and ground noise. In stacking power gating technique two transistors ST1 and ST2 are connected to virtual ground of the circuit to reduce the magnitude of voltage glitches and current but this design results in increase in delay and area.

3. Proposed Approximate Adder

We have presented three designs of approximate adders, which are explained in the subsequent section of the paper.

3.1 1-BIT APPROXIMATION_1

First proposed approximate adder is shown in figure 1. It is designed using total 8 number of transistors. The 1-bit approximation_1 has C_{out} = B for 7 cases out of 8 cases, except A = 1, B = 0, C =1. This approximate adder has total 4 errors, 1 error in C_{out} and 3 errors in Sum.

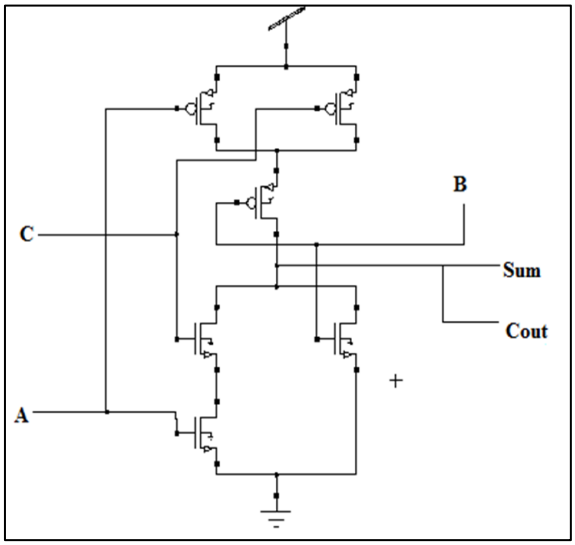

Figure 1: 1-bit approximation_1

3.2 1-BIT APPROXIMATION_2

Figure 2 shows the design of proposed 1-bit approximation_2. The 1-bit approximation_2 has Cout= A for 7 cases out of 8 cases, except A =0, B =1, C =1. It has total 4 errors, 1 error in Cout and 3 errors in Sum.

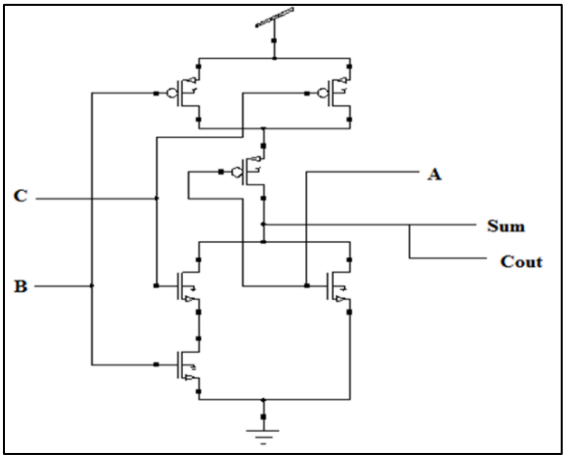

Figure 2: 1-bit approximation_2

3.2 1-BIT APPROXIMATION_3

The circuit diagram of 1-bit approximation_3 is shown in fig. 3. In this fig. Cout = C for 7 cases out of 8 cases, except A =1, B =1, C =0. It has total 4 errors; one error is in Cout and three errors in Sum.

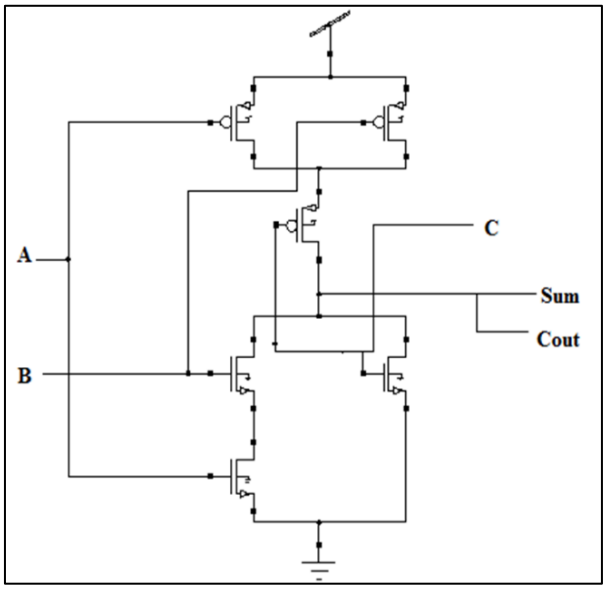

Figure 3: 1-bit approximation_3

All the three circuit of proposed approximate adders are designed for low leakage and lesser energy consumption which is having following features:

1. All the proposed approximate adders are having maximum four errors in the output of full adder. According to literature errors upto four or five are acceptable and can be successfully used in various image processing applications.
2. Approximate adder shown in fig. has very small critical path from input to output which in turns reduces the delay and hence the energy consumption.
3. In all the proposed approximate adders shown in fig. respectively needs very less MOS transistors as compared to the accurate adders which reduces the leakage power consumption.

3.3 TRANSISTOR SIZING

This methodology guarantees that only the right transistors (the ones in the critical path) are sized and in a proper way. No oversizing or under sizing will be incurred, which makes it optimal for power-delay product performance. Sizing of the transistors for any circuit is done in an iterative manner by the following steps:

1. Set all transistors (N and P) to the maximum size.
2. Simulate the circuit with all possible input-pattern-to-input-pattern transitions.
3. Figure the transition with the highest delay and mark the transistors that are involved.
4. Size one of the transistors that are involved.
5. Repeat steps 2, 3, and 4, until the PDP for the cell continues to increase.
6. Record the transistor sizes corresponding to the minimum PDP.

4. SIMULATION RESULTS

The simulations of all the existing and proposed approximate adder circuit are performed using HSPICE EDA tool. All the results are presented at 45nm CMOS technology. 45nm technology file is referred from predictive technology model (PTM). To measure the average power we have chosen the frequency of 500 MHz. We have chosen the latest input pattern for average and delay measurement which covers all the possible worst case of the circuit and gives the maximum possible value of delay and average power dissipation in existing and proposed approximate adder circuits.

Table 1: Comparison between average power consumption and delay of proposed and one bit approximate adder

500 MHz		
Circuit name	**Average Power in (uw)**	**Delay In (ps)**
Existing_approximate_adder_1	5.58E-06	2.88E-10
Existing_approximate_adder_2	5.41E-06	3.27E-10
Existing_approximate_adder_3	5.25E-06	3.75E-10

Existing_approximate_adder_4	5.11E-06	4.23E-10
proposed_approximate_adder_1	3.25E-06	3.33E-09
proposed_approximate_adder_2	3.12E-06	3.36E-09
proposed_approximate_adder_3	3.05E-06	3. 37E-09

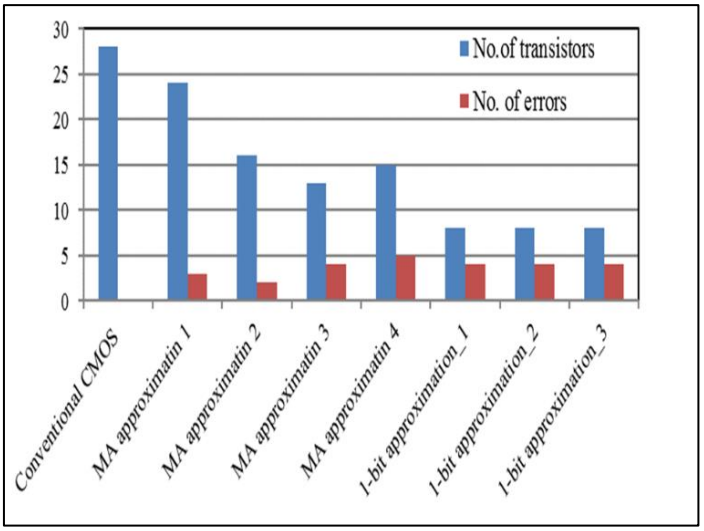

Figure 4: Comparison of number of transistors of 1-bit existing and proposed approximate adder

Figure 4 shows the comparison of number of transistors and number of approximate outputs among the various proposed and existing approximate adders. It is clearly concluded from the figure 4 that proposed approximate adders saves large silicon area. Figure 5 shows the comparison of leakage power consumption among the proposed and existing approximate adder.

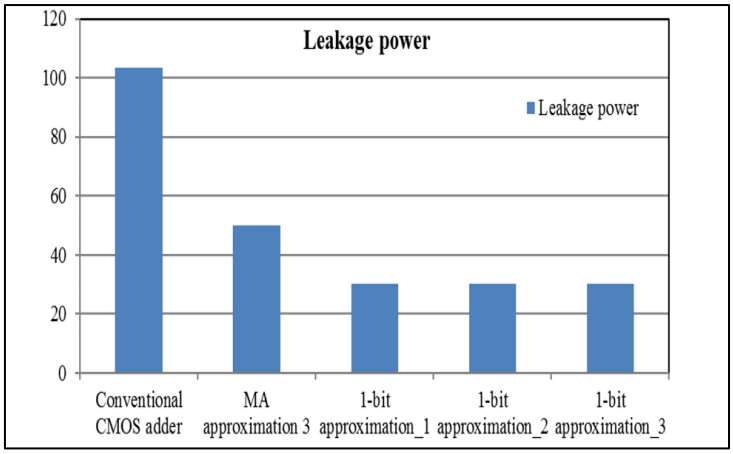

Figure 5: Comparison of leakage power of 1-bit existing and proposed approximate adder

Table 2: Comparison of complete performance parameters among 1-bit existing and proposed approximate adder at 1.1V, 27C temperature at 45nm technology

Name of adder	No. of transistor used	Average power (µw)	Leakage power (pw)	Peak power (µw)	Delay (ns)	PDP (fj)
Conventional CMOS	28	5.797	103.28	84.98	0.523	3.036
MA approximation 1	24	4.394	78.55	77.95	0.282	1.241
MA approximation 2	16	3.494	73.45	51.26	0.316	1.107
MA approximation 3	13	3.312	49.75	43.38	0.467	1.549
MA approximation 4	15	3.350	50.95	51.59	0.416	1.396
1-bit approximation_1	8	2.411	29.95	38.92	0.239	0.576
1-bit approximation_2	8	1.603	29.85	35.30	0.284	0.455
1-bit approximation_3	8	0.960	29.90	35.32	0.261	0.250

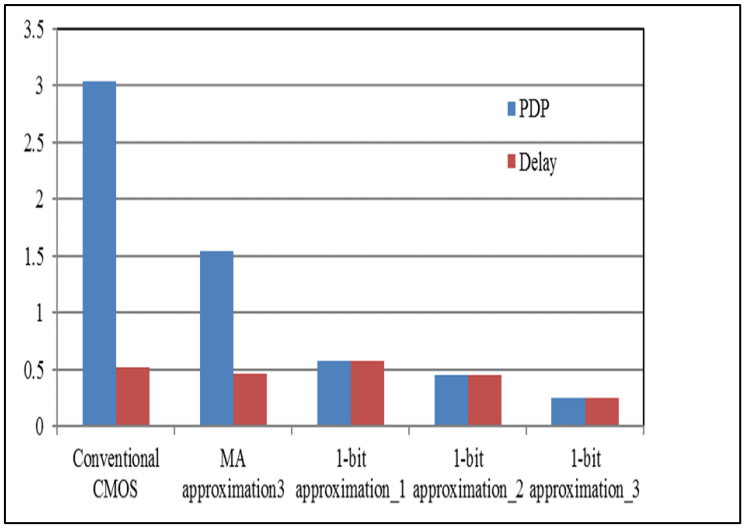

Figure 6: Comparison of delay and PDP of 1-bit existing and proposed approximate adder

Table 2 shows the comparison among the existing and proposed approximate adders for all the possible performance parameters. It is clear from the table 2 that all the proposed approximate adders are having best leakage power and PDP as compared to the existing adders. Figure 6 shows the comparison among PDP of the entire proposed and existing approximate adder.

6. CONCLUSION

The three modified 1-bit approximate adders have designed in this thesis. A detailed comparison of various parameters between existing and proposed approximate adders is presented in the result section of the thesis. In proposed approximate adders, number of transistors is lesser as compared to the existing approximate adder as well as conventional adder. It saves 71% silicon area as compared to the existing approximate adder. Similarly, leakage power reduces upto 70% as compared to the existing design of approximate adder. A result of PDP is also shown reduction as compared to the conventional as well as existing approximate adder. All the performance parameters show improvement as compared to existing design in the literature view.

Future Scope

One can extend this work at higher frequency upto 2GHz. Frequency. Also this work can be extended for novel devices like carbon nano tubes field effect transistor (CNTFET), tunnelling FET (TFET) etc. This work can be extended to use for other low power applications as well as for reduction in ground bounce noise

REFERENCES

1. Amin, B., Member, I., Alireza, M., & Jelveh, J. (2012). Low power full adder using 8T structure. *Proceeding of the international multi conference of engineers and computer scientists*, 2, 1190-1194.
2. Sudsakorn, A., Tooprakai, S., & Dejhan, K. (2012, May). Low power cmos full adder cells. In *2012 9th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology* (pp. 1-4). IEEE.
3. Candy, G., & Savinder, K. (2016). Design and analysis of low leakage one bit adder for inexact computing. *An International Journal of Engineering Sciences*, 20, 150-155.
4. Alam, I., & Lau, K. T. (2017). Approximate adder for low-power computations. *International Journal of Electronics Letters*, *5*(2), 158-165.
5. Geetha, S., & Amritvalli, P. (2017). High Speed Error Tolerant Adder for Multimedia Applications. *J. Electron Test*. doi: 10.1007/s10836-017-5680.
6. Alam, I. (2016). Approximate adder for low-power computations. *International Journal of Electronics Letters.*
7. Guan, Z. (1993). A simple and high speed CMOS carry chain adder architecture. *International Journal of electronics*, 75(4), 743-752.
8. Singh, R. (2014). Modelling and analysis of low power 10T full adder with reduced ground bounce noise. *Journal of circuits, systems and computers*, 23(1), 145005.